PROGRAMMED I/O ETHERNET ADAPTER WITH EARLY INTERRUPTS
FOR ACCELERATING DATA TRANSFER

ABSTRACT OF THE DISCLOSURE

5   In a Local Area Network (LAN) system, an ethernet
adapter exchanges data with a host through programmed I/O (PIO)
and FIFO buffers. The receive PIO employs a DMA ring buffer
backup so incoming packets can be copied directly into host
memory when the PIO FIFO buffer is full. The adapter may be
10   programmed to generate early receive interrupts when only a
portion of a packet has been received from the network, so as
to decrease latency. The adapter may also be programmed to
generate a second early interrupt so that the copying of a
large packet to the host may overlap reception of the packet
15   end. The adapter to begin packet transmission before the
packet is completely transferred from the host to the adapter,
which further reduces latency. The minimal latency of the
adapter allows it to employ receive and transmit FIFO buffers
which are small enough to be contained within RAM internal to
20   an Application Specific Integrated Circuit (ASIC) containing
the transceiver, ethernet controller, FIFO control circuitry
and the host interface as well.

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